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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/767,449	01/30/2004	Fubito Igari	008312-0308038	3937

909 7590 01/17/2007  
PILLSBURY WINTHROP SHAW PITTMAN, LLP  
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MCLEAN, VA 22102

EXAMINER
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DAVIDSON, DAN

ART UNIT	PAPER NUMBER
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2627

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/17/2007	PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

**Office Action Summary**

Application No.

10/767,449

Applicant(s)

IGARI, FUBITO

Examiner

Dan I. Davidson

Art Unit

2627

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 January 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 1-6 and 17-20 is/are allowed.
- 6) ☒ Claim(s) 7-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some \* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date 01302004; 11302004; 03212006.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: \_\_\_\_\_.

### **DETAILED ACTION**

1. The information disclosure statements filed January 30, 2004; November 30, 2004; and March 21, 2006 have been received and have been considered and made of record.

### ***Specification***

2. The disclosure is objected to because of the following informalities:

(1) On page 7, line 9 and on page 21, line 22, "serve" should be replaced with --servo--.

(2) On page 18, line 1, "WG2a" should be replaced with --WG1a--.

(3) On page 20, line 16, "negated" should be replaced with --asserted--.

Appropriate correction is required.

### ***Claim Rejections - 35 USC § 112***

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 7-16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Re claim 7; this claim conflates the embodiments of Figures 2 and 5 (defining Figure 2 as "the first mode" and Figure 5 as "the second mode") and is therefore indefinite. Claims 1 and 2, from which claim 7 depends, are drawn specifically to the embodiment in Figure 2 to the exclusion of the embodiment in Figure 5. Claim 1 recites that the external circuit outputs a second write gate signal and that a write inhibition

controller monitors the second write gate signal, limitations that are drawn to the embodiment of Figure 2 to the exclusion of the embodiment in Figure 5.

***Allowable Subject Matter***

5. Claims 1-6 and 17-20 are allowed over the prior art of record.

Re claim 1; the prior art of record, and in particular Applicant's Admitted Prior Art (AAPA) and Ogawa et al (JP-2000298934-A), fails to teach or suggest all of the claimed limitations in combination, specifically including the limitation that a write inhibition controller monitors the second write gate signal input via the second terminal, and detects, as a write inhibition state, a state in which writing of data to the disk is dictated during a period in which writing of data to the disk should be inhibited.

Re claim 19; the prior art of record, and in particular Applicant's Admitted Prior Art (AAPA) and Ogawa et al (JP-2000298934-A), fails to teach or suggest all of the claimed limitations in combination, specifically including the limitations that a write inhibition controller monitors the second write gate signal input via the second terminal, and detects, as a write inhibition state, a state in which writing of data to the disk is dictated during a period in which writing of data to the disk should be inhibited, the write inhibition controller outputting the second write gate signal as the fourth write gate signal in a normal state without changing a state of the second write gate signal, the write inhibition controller negating the second write gate signal and outputting the negated second write gate signal as the fourth write gate signal in the write inhibition state; and a head amplifier circuit which causes a head to write, to the disk, the write

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data processed by the signal processing circuit in accordance with the fourth write gate signal output through the third terminal of the disk controller.

Re claim 20; the prior art of record, and in particular Applicant's Admitted Prior Art (AAPA) and Ogawa et al (JP-2000298934-A), fails to teach or suggest all of the claimed limitations in combination, specifically including the limitations of outputting a second write gate signal corresponding to the first write gate signal from the signal processing circuit to the disk controller, the second write gate signal reflecting a signal delay in the predetermined signal processing; detecting, as a write inhibition state, a state in which an instruction to write data to the disk is issued during a period in which writing of data to the disk should be inhibited, in accordance with the second write gate signal output from the signal processing circuit to the disk controller; and outputting, from the disk controller to the head amplifier circuit, the second write gate signal as a fourth write gate signal in a normal state, without changing a state of the second write gate signal, the fourth write gate signal instructing writing, to the disk, of the write data processed by the signal processing circuit; and negating the second write gate signal in the write inhibition state, and outputting, from the disk controller to the head amplifier circuit, the negated second write gate signal as the fourth write gate signal in the write inhibition state.

### ***Conclusion***

6. The following cited art is not prior art but is being cited since it is pertinent to applicant's disclosure.

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Sai et al (US 2006/0171053 A1) teach a disk drive in which a disk controller outputs to a R/W channel data indicating data length of data to be transferred in order to prevent erroneous writing resulting from a mismatch in timing between the disk controller and the R/W channel.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dan I. Davidson whose telephone number is (571) 272-7552. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Andrea L. Wellington can be reached on (571) 272-4483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DID  
Dan I Davidson  
January 8, 2007

  
ANDREA WELLINGTON  
SUPERVISORY PATENT EXAMINER